Voltage Controlled Logic-in-memory Architecture in Manganite Nanowire

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Introduction

In-memory computing has been a hot research field nowadays and shows potential to overcome the Von Neumann bottleneck in conventional computers. However, most proposed designs demand the key usage of electrical current which will generate substantial heat and power consumption when miniaturized. Here, we show an example by exploiting electric field effect to achieve a logic-in-memory architecture in manganite nanowire.

Experiments

$La_{1-x}Ca_xMnO_3$ (x = 0.15) thin films (30 nm) were grown on single crystal $SrTiO_3$ (001) substrates by pulsed laser deposition (248 nm, 1 J cm^{-2} fluence, 2Hz) at 780 ℃ in 5×10^{-5} mbar of oxygen (with 10% ozone mixture). Electron beam lithography, Electron beam evaporation, Argon ion beam etching and UV contact lithography was applied to fabricate LCMO nanowires and side gate.

STO substrate
↓ PLD
LCMO film
↓ EBL+ E-beam
Au markers
↓ EBL+ Ar ion beam
LCMO nanowires
↓ UV lithography
Side gate

Results & Discussion

Device geometry and electric field effects

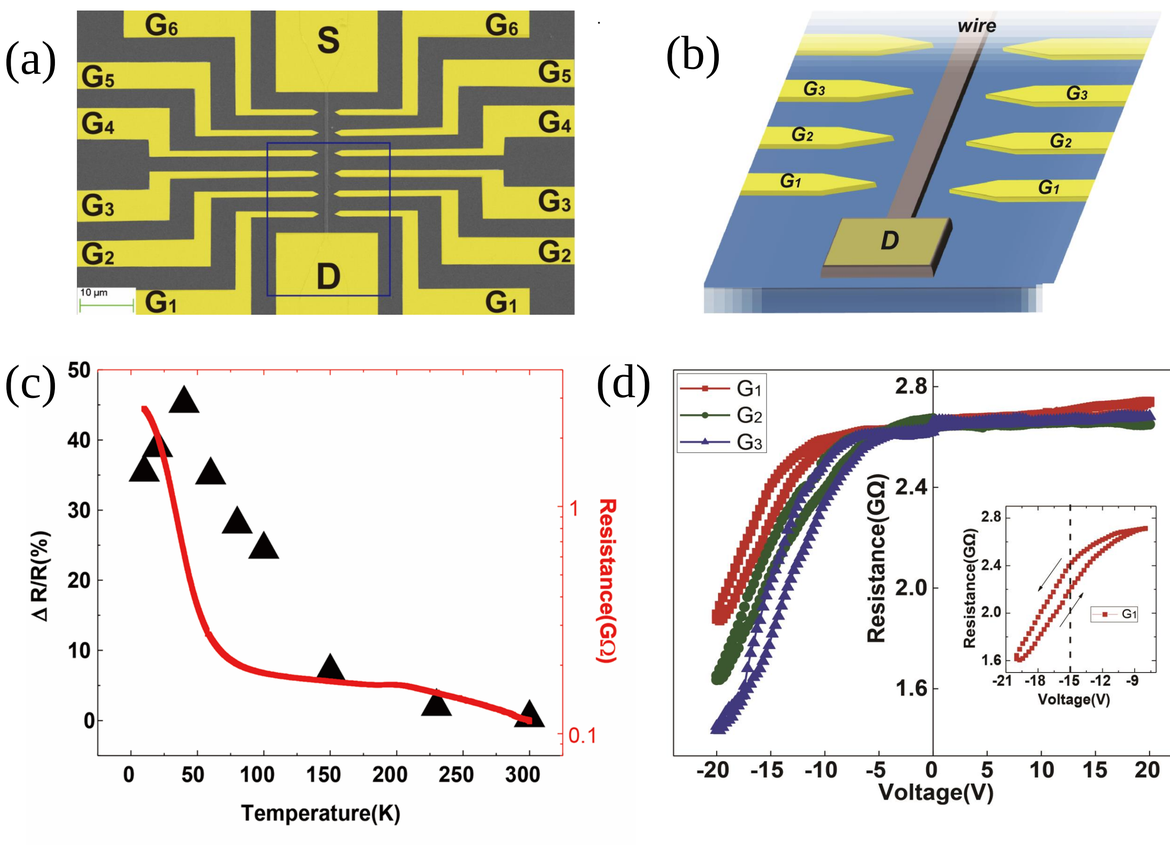


Fig. 1 (a) The SEM image of device configuration. (b) A magnified schematic showing the electric field effect in LCMO induced by different pairs of lateral gates. (c) Resistance vs temperature curve (red) under 0 V gate voltage. The relative percentage of resistance change vs temperatures (black triangles). (d) Resistance vs gate voltage curves for 3 pairs of lateral gates operating individually.

There are several advantages to this type of device structure. Using pure electric field manipulating can greatly reduce the power consumption of the device. It provides the necessary conditions to achieve multi-bit memory.

Multilevel memory

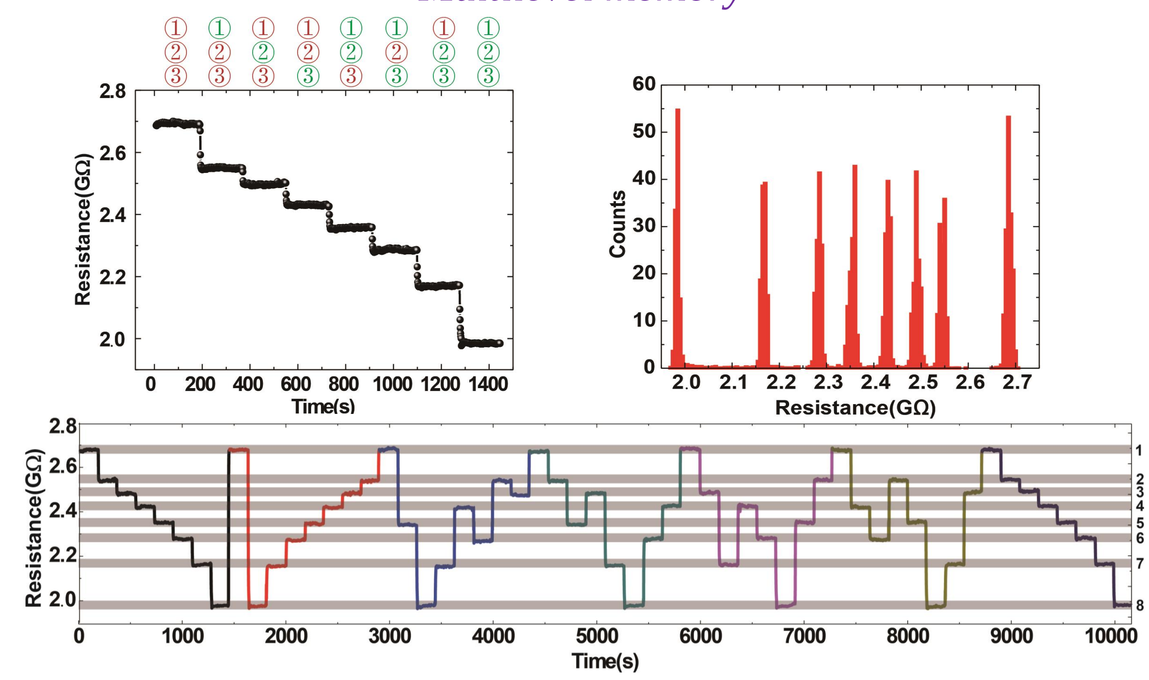
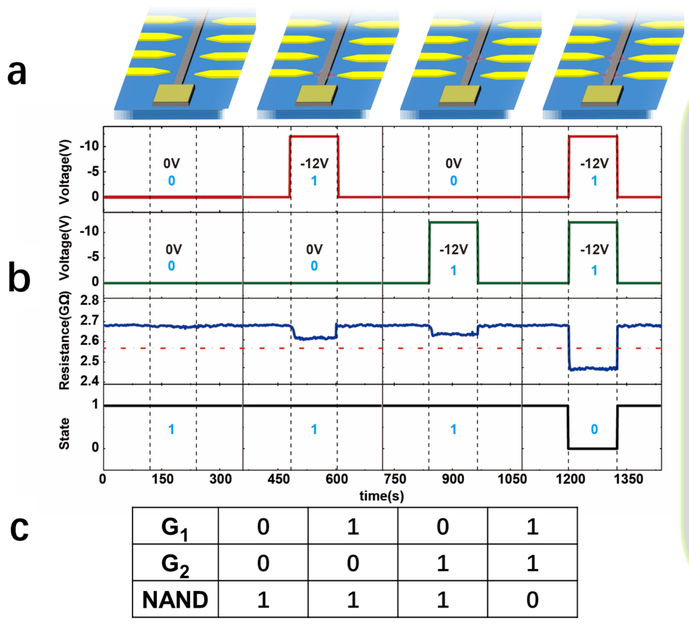


Fig. 2 (a) Eight-level resistive behavior at 10K. Green and red circles represent the gate voltage in on and off state, respectively (b) Repeatable multi-level switching by randomly controlling the voltage on and off of three pairs of gates. (c) Histogram of eight clearly distinguishable resistive levels.

The very same LCMO nanowire device can be used to carry out "NAND" and "NOR" Boolean logic operations.

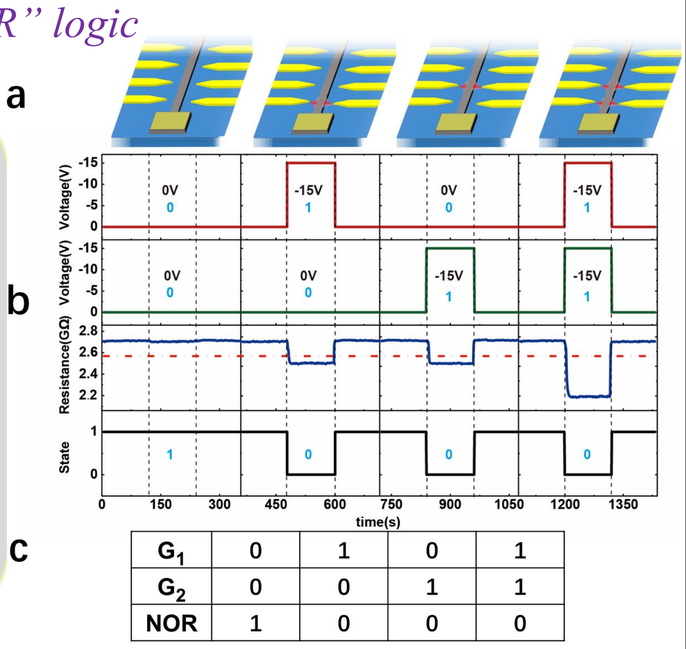
"NAND" logic



G_1	0	1	0	1
G_2	0	0	1	1
NAND	1	1	1	0

Fig. 3 (a) Illustration of logic NAND input combination by selectively turning on the local gate biases. (b) Experimental results obtained on the device demonstrating the NAND operation. The judgment resistance is set at 2.57 GΩ . (c) The truth table of NAND operation..

"NOR" logic



G_1	0	1	0	1
G_2	0	0	1	1
NOR	1	0	0	0

Fig. 4 (a) Illustration of logic NOR input combination by selectively turning on the local biases. (b) Experimental results obtained on the device demonstrating the NOR operation. The judgment resistance is set at 2.57 GΩ. (c) The truth table of NOR operation.

Switching time ~ 8ns

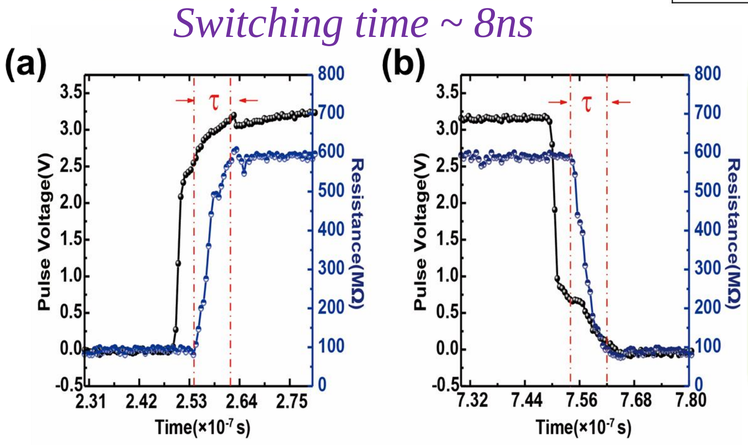


Fig. 4 The switching time measurement under pulse voltage of LCMO nanowire device. (a) the rising edge. (b) the falling edge. Switching time approximately of 8 ns.

conclusion

We successfully demonstrated that multi-bit memory and logic operation can be integrated into a single manganite nanowire device unit. The fact that localized electric field can regulate macroscopic transport properties ensures that the device requires 4 orders of magnitude smaller current density for operation comparing to previous devices with similar functionality, which greatly reduces the power consumption and improves the device stability. This, along with the fast switching time (~8 ns), warrants the practical low power switching applications of the device.